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ATTORNEY DOCKET NO. 70011377-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Sai-Mun Lee, et al.

Serial No.: 10/649,006 Examiner: Nadav, Ori

Filing Date: August 26, 2003 Group Art Unit: 2811

Title: SEMICONDUCTOR PACKAGING STRUCTURE

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on November 16, 2005 .

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) **$500.00**.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)(1)-(5)) for the total number of months checked below:

☐	one month	$ 120.00
☐	two months	$ 450.00
☐	three months	$1020.00
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☐ The extension fee has already been filled in this application.

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **50-3718** the sum of $500.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-3718** pursuant to 37 CFR 1.25.

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☒ I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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☐ I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Date of Facsimile:

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Signature

Respectfully submitted,

Sai-Mun Lee, et al.

By James A. Sheridan 01/17/06

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl. No.	:	10/649,006	Confirmation No. 5926
Appellant	:	Sai-Mun Lee, et al.	
Filed	:	August 26, 2003	
TC/A.U.	:	2811	
Examiner	:	Nadav, Ori	
Docket No.	:	70011377-2	

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
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APPEAL BRIEF

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APPEAL BRIEF

Dear Sir:

This Appeal Brief is submitted in response to the Examiner's Final Office Action dated August 16, 2005.

Appellants filed a Notice of Appeal on November 16, 2005.

Real Party in Interest

The real party in interest is Avago Technologies General IP (Singapore) Pte. Ltd. (Company Registration No. 200512430D), a company incorporated under the laws of Singapore whose registered office is at 8 Cross Street, #11-00 PWC Building, Singapore 048424.

Related Appeals and Interferences

There are no related appeals and/or interferences.

Status of Claims

Claims 1, 2, 5-7, 9 and 11-18 are pending, all of which stand rejected.

A copy of the claims is attached as a Claims Appendix to this Appeal Brief.

Status of Amendments

No amendments were made to the claims subsequent to final rejection. All amendments have been entered.

Summary of Claimed Subject Matter

In one embodiment (claim 1), a packaging structure (p. 7, lines 1-4; FIG. 2, 30) for a semiconductor device (p. 8, lines 19-28; FIG. 2, 34) comprises a substrate (p. 7, lines 6-10; FIG. 2, 32) that is surface-mountable on a mounting surface of a circuit board. The substrate has a first side (FIG. 2, 44) facing away from the mounting surface and a second side (FIG. 2, 46) being on the same side of the structure as the mounting surface. The substrate is hollow (p. 7, lines 12-15; FIG. 2), with the hollow extending from the first side of the substrate to the second side of the substrate. A recess (FIG. 2, 48) is provided in the second side of the substrate. A semiconductor die has a first side and a second side is mounted in the recess, with the first side of the semiconductor die facing away from the mounting surface, and a portion of the first side of the semiconductor die bonded to the substrate within the recess by electrically conductive bonding pads (p. 8, line 30 - p. 9, line 9; FIG. 2, 76).

Grounds of Rejection to be Reviewed on Appeal

1. Whether claims 1, 2, 5-7, 9 and 11-18 should be rejected under 35 USC 112, 1st paragraph, as failing to comply with the written description requirement.

2. Whether claims 1, 2, 9, 11 and 12 should be rejected under 35 USC 102(b) as being anticipated by Nicewarner, Jr. (US Pat. No. 5,327,325).

3. Whether claims 5-7 and 16-18 should be rejected under 35 USC 103(a) as being unpatentable over Nicewarner, Jr. (US Pat. No. 5,327,325) in view of Peterson et al. (US Pat. No. 6,674,159 B1).

4. Whether claims 13-15 should be rejected under 35 USC 103(a) as being unpatentable over Nicewarner, Jr. (US Pat. No. 5,327,325) in view of Bhagwagar (US Pat. No. 6,791,839 B2).

Argument

1. Whether claims 1, 2, 5-7, 9 and 11-18 stand rejected under 35 USC 112, 1st paragraph, as failing to comply with the written description requirement.

a. Claims 1, 2, 5, 9 and 11-18

With respect to claim 1, the Examiner asserts:

> . . .The specification recites a first hollow extending from the first side of the substrate to a die and a second hollow (recess) extending from the die to the second side of the substrate. There is no support in the specification for a hollow extending from the first side of the substrate to the second side of the substrate, as recited in claim 1.

8/16/2005 Final Office Action, p. 3, lines 1-5.

Appellants respectfully disagree. Appellants' specification states:

> The hollow within the substrate is made up of a first recess 42, in the first major side 44 and a second recess 48 in the second major side 46 (the underside in the orientation of Figure 2), meeting within the substrate.

Specification, p. 7, lines 12-14.

In light of this description, appellants believe the following language of their claim 1 finds support in their specification:

> a substrate. . ., wherein the substrate has a first side facing away from the mounting surface and a second side being on the same side of the structure as the mounting surface, and wherein the substrate is hollow, with the hollow extending from the first side of the substrate to the second side of the substrate;

Appellants therefore believe the rejection of claims 1, 2, 5, 9 and 11-18 under 35 USC 112, 1st paragraph, should be withdrawn.

b. Claims 6 and 7

Apellants' claim 6 provides the following additional description regarding the "hollow" of claim 1, reciting:

> wherein the second substrate layer [introduced in claim 5] has inner walls defining a hollow portion extending from the first side of the second substrate layer to the second side of the second substrate layer, with the inner walls defining at least part of said recess and said hollow.

As a result of the description of the "hollow" in claim 1 (the parent claim of claim 6), as well as the above additional description of the "hollow", appellants ask the Examiner to withdraw the rejection of claims 6 and 7 under 35 USC 112, 1st paragraph.

2. Whether claims 1, 2, 9, 11 and 12 stand rejected under 35 USC 102(b) as being anticipated by Nicewarner, Jr. (US Pat. No. 5,327,325; hereinafter "Nicewarner").

a. Claims 1, 11 and 12

Appellants' claim 1 recites:

> 1. A packaging structure for a semiconductor device, comprising:
> a substrate surface-mountable on a mounting surface of a circuit board, wherein the substrate has a first side facing away from the mounting surface and a second side being on the same side of the structure as the mounting surface, and wherein the substrate is hollow, with the hollow extending from the first side of the substrate to the second side of the substrate;
> a recess in the second side of the substrate;
> a semiconductor die having a first side and a second side, and mounted in said recess, with the first side of the semiconductor die facing away from the mounting surface and a portion of the first side of the semiconductor die bonded to said substrate within the recess by electrically conductive bonding pads.

With respect to appellants' claim 1, the Examiner asserts that Nicewarner teaches:

> . . .a packaging structure for a semiconductor device, comprising:
> a substrate surface-mountable on a mounting surface of a circuit board, wherein the substrate 12 has a first side facing away from the mounting surface and a second side being on the same side of the structure as the mounting surface, and wherein the substrate is hollow 22, with the hollow 22 extending from the first side of the substrate 12 to the second side of the substrate;
> a recess (the recess within and below resin 80) in the second side of the substrate;
> a semiconductor die 26, 28 having a first side and a second side, and mounted in said recess, with the first side of the semiconductor die facing away from the mounting surface and a portion of the first side of the semiconductor die bonded to said substrate within the recess by electrically conductive bonding pads 71.
>
> 8/16/2005 Final Office Action, pp. 3-4.

Appellants respectfully disagree. To begin, appellants do not believe that Nicewarner's substrate 12 is "surface-mountable on a mounting surface of a circuit board". Rather, Nicewarner's package 10 is only mountable via leads 58, 62. That is, the lower flat surface 16 of Nicewarner's substrate 12 is not "surface-mountable". Nor is Nicewarner's lower mounting surface 52 "surface-mountable on a mounting surface of a circuit board", as the mounting surface 52 is substantially covered by a lid member 56. Nor does the lid member 56 appear to be "surface-mountable on a mounting surface of a circuit board". Nicewarner certainly doesn't indicate that it is, and the height differential between the lower surface of the lid member 56 and the lower surfaces of the leads 58, 62 supports appellants' position that the lid member 56 is not a "surface-mountable" part of the substrate 12.

Next, it is noted that Nicewarner's "substrate support member 12. . .has an upper substantially flat surface 14 and a lower substantially flat surface 16." *See*, Nicewarner, col. 4, lines 9-11. The "recess 22 is located around the entrance to the cavity 18 in the upper flat surface 14 of the base substrate support member 12 and another substantially identical substantially rectangular shaped recess 24 is located around the entrance to the cavity 20 in the lower flat surface 16 of the base substrate

support member 12." *See*, Nicewarner, col. 4, lines 19-24. However, "[t]he two cavities 18 and 20 are separated by a partition 21 that is part of the substrate support member 12." *See*, Nicewarner, col. 4, lines 16-18. Thus, the Examiner's assertion that Nicewarner discloses a "hollow 22 extending from the first side of the substrate 12 to the second side of the substrate" is wholly unsupported by Nicewarner's teachings. Furthermore, it does not appear that Nicewarner's partition 21 could be easily removed, as "flip-chip solder bond connections 71 and 73" bond the "chips 28 and 30" to the "partition 21". *See*, e.g., Nicewarner, col. 5, lines 1-13.

In the Advisory Action dated October 28, 2005, the Examiner counters Applicants' above position by stating:

> The examiner does not consider cavity 20 as part of the "hollow". Only cavity 18 is considered as part of the "hollow". The second side of substrate 12 is taken to be the lower surface of the layer having sidewalls 60 and 64, and surface 52. Partition 21 is therefore located below the second side of the "considered substrate 12". Therefore, Nicewarner teaches a "hollow 22 extending from the first side of the substrate 12 to the second side of the substrate", as claimed.
>
> 10/28/2005 Advisory Action, pp. 3-4.

It is noted that Nicewarner discloses a substrate 12 having an upper surface 14 and a lower surface 16 (see FIG. 3). Although FIG. 3 seems to show that the substrate 12 is comprised of several parts, including the partition 21, Nicewarner does not specifically reference or discuss these other parts. Rather, Nicewarner merely discloses a substrate 12 that includes all of the parts. In his Advisory Action, the Examiner tries to single out the upper component of the substrate 12, and construe this one component as being equivalent to the "substrate" of appellants' claim 1. However, Nicewarner does not support a singling out of one component of the substrate 12. Furthermore, even assuming, arguendo, that it is proper to single out the upper component of the substrate 12 as a *substrate* by itself, this would result in the singled out *substrate* not being "surface-mountable on a mounting surface of a circuit board", which is also an element of appellants' claim 1.

Appellants' claim 1 is believed to be allowable over Nicewarner's teachings for

at least the above reasons.

Appellants' claims 9, 11 and 12 are believed to be allowable at least for the reason that they depend from claim 1.

b. Claim 2

Appellants' claim 2 recites:

> 2. A structure according to claim 1, wherein said recess includes an exposed portion of the substrate facing the mounting surface and said portion of the first side of the semiconductor die is bonded to said exposed portion.

With respect to claim 2, the Examiner asserts that, "Nicewarner Jr. teaches in figure 3 and related text a recess includes an exposed portion of the substrate facing the mounting surface and said portion of the first side of the semiconductor die is bonded to said exposed portion." *See*, 8/16/2005 Final Office Action, p. 4. However, to support this rejection, the Examiner must 1) equate the "substrate" of appellants' claim 2 with all of Nicewarner's substrate 12, and 2) equate the "semiconductor die" of appellants' claim 2 with Nicewarner's die 30 or 32. Yet, in rejecting appellants' claim 1 (the parent of appellants' claim 2), and in an attempting to identify the "hollow" of appellants' claim 1, the Examiner construes appellants' substrate as being equivalent to only the *upper component* of Nicewarner's substrate 12. Appellants' claim 2 is therefore believed to be allowable because it depends from claim 1, and because the Examiner's positions in rejecting claim 1 and claim 2 are at odds with each other.

3. Whether claims 5-7 and 16-18 stand rejected under 35 USC 103(a) as being unpatentable over Nicewarner, Jr. (US Pat. No. 5,327,325; hereinafter "Nicewarner") in view of Peterson et al. (US Pat. No. 6,674,159 B1; hereinafter "Peterson").

Appellants' claims 5-7 and 16-18 are believed to be allowable at least for the reason that they depend from appellants' claim 1, and because Peterson fails to disclose that which appellants have already shown is missing from Nicewarner. *See*, Section 2 of this Argument, *supra*.

Furthermore, appellants can find no suggestion or motivation to combine Nicewarner's and Peterson's teachings, as the incorporation of Peterson's hollow into Nicewarner's package would appear to defeat the purpose of Nicewarner's invention, which is to provide a package that can carry *multiple* chips.

4. Whether claims 13-15 stand rejected under 35 USC 103(a) as being unpatentable over Nicewarner, Jr. (US Pat. No. 5,327,325; hereinafter "Nicewarner") in view of Bhagwagar (US Pat. No. 6,791,839 B2).

With respect to appellants' claim 13, the Examiner asserts that Nicewarner discloses the presence of an encapsulant (believed to be encapsulant 80 in FIG. 3) that is "flush" with the level of the second side of the substrate". Appellants respectfully disagree.

Nicewarner's resin material 80 encapsulates "flip-chip solder bond connections 71 and 73", which are not flush with the substrate that holds chips 28 and 30. Appellants' claim 13 is believed to be allowable for at least this reason, and because Peterson fails to disclose that which appellants have already shown is missing from Nicewarner. *See*, Section 1 of these Remarks/Arguments, *supra*.

Appellants' claims 14 and 15 are believed to be allowable at least for the reason that they depend from claim 13.

5. Conclusion

In summary, the art of record does not teach nor suggest the subject matter of Appellants' claims 1, 2, 5-7, 9 and 11-18. These claims are therefore believed to be allowable.

Respectfully submitted,
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Appendix

Claim 1 (previously presented): A packaging structure for a semiconductor device, comprising:

a substrate surface-mountable on a mounting surface of a circuit board, wherein the substrate has a first side facing away from the mounting surface and a second side being on the same side of the structure as the mounting surface, and wherein the substrate is hollow, with the hollow extending from the first side of the substrate to the second side of the substrate;

a recess in the second side of the substrate;

a semiconductor die having a first side and a second side, and mounted in said recess, with the first side of the semiconductor die facing away from the mounting surface and a portion of the first side of the semiconductor die bonded to said substrate within the recess by electrically conductive bonding pads.

Claim 2 (previously presented): A structure according to claim 1, wherein said recess includes an exposed portion of the substrate facing the mounting surface and said portion of the first side of the semiconductor die is bonded to said exposed portion.

Claims 3 & 4 (canceled)

Claim 5 (original): A structure according to claim 1, wherein:

said substrate comprises first and second substrate layers, the first substrate layer having first and second opposing sides and the second substrate layer having first and second opposing sides;

the first side of the first substrate layer is the first side of the substrate and the second side of the second substrate layer is the second side of the substrate; and

the second side of the first substrate layer is mounted to the first side of the second substrate layer.

Claim 6 (previously presented): A structure according to claim 5, wherein the second substrate layer has inner walls defining a hollow portion extending from the first side of the second substrate layer to the second side of the second substrate layer, with the inner walls defining at least part of said recess and said hollow.

Claim 7 (previously presented): A structure according to claim 6, wherein:

the first substrate layer has a hollow portion, coincident with the hollow portion of the second substrate layer, extending from the first side of the first substrate layer to the second side of the first substrate layer;

the hollow portion through the first substrate layer is smaller than the hollow portion through the second substrate layer, such that where the second side of the first substrate layer is mounted to the first side of the second substrate layer, a portion of the second side of the first substrate layer is exposed, not being covered by the first side of the second substrate layer; and

the exposed portion of the first substrate layer defines at least part of the recess.

Claim 8 (canceled)

Claim 9 (original): A structure according to claim 1, further comprising electrical connections running from where the die is bonded to said recess to the mounting surface.

Claim 10 (canceled)

Claim 11 (currently amended): A structure according to claim 1, wherein said semiconductor die has edges, and further comprising sealant between the edges of said semiconductor die and said substrate.

Claim 12 (original): A structure according to claim 11, wherein said sealant comprises a highly viscous material.

Claim 13 (original): A structure according to claim 1, further comprising a thermally conductive and electrically insulating encapsulant in said recess, on the second side of the semiconductor die.

Claim 14 (previously presented): A structure according to claim 13, wherein said encapsulant comprises a viscous material.

Claim 15 (original): A structure according to claim 14, wherein the encapsulant is flush with the level of the second side of the substrate.

Claim 16 (previously presented): A structure according to claim 1, wherein said semiconductor die is a sensor chip.

Claim 17 (original): A structure according to claim 1, further comprising a non-opaque portion mounted to the substrate on the same side of the structure as the first side of the substrate.

Claim 18 (original): A structure according to claim 17, wherein said non-opaque portion is a transparent cover on the first side of the substrate.

Evidence Appendix

None.

Related Proceedings Appendix

None.